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EXAMINER	
VOELTZ, EMANUEL T	

ART UNIT	PAPER NUMBER
2121	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/135,405	REISS ET AL.	
	Examiner	Art Unit	
	Emanuel T. Voeltz	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *All*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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Examiner's Detailed Office Action

This action is in response to an amendment filed on May 1, 2002

Claims 1-70 have been examined.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on May 1, 2002, October 22, 2002, November 19, 2002, January 2, 2003, April 25, 2003, July 3, 2003, October 9, 2003, December 18, 2003 and March 29, 2004 are all in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1,3-15,17-31,33-45,58,60-65,67-70 are rejected under 35 U.S.C. 102(e) as being anticipated by US patent 6,556,881 B1 granted to Miller.

Regarding claim 1,

A method for processing wafers in a manufacturing execution system using a run-to-run controller with a fault detection system (see column 3, lines 63-67), said method comprising the steps of:

1) receiving, into said run-to-run controller, a recipe for controlling a tool, wherein said recipe includes at least one setpoint for obtaining one or more target wafer properties (see column 5, lines 24-37, batch [i.e. wafer-to-wafer or lot-to-lot]);

2) monitoring processing of said wafers by measuring processing attributes including wafer properties and fault conditions identified by said fault detection system (see Figure 1, sensor 115, column 3, lines 5-15);

3) forwarding said processing attributes to said run-to-run controller (see column 5, lines 57-67 and column 6, lines 1-3); and

4) modifying said at least one setpoint of said recipe at said run-to-run controller according to said measured processing attributes to maintain said target wafer properties, except when a fault condition is detected by said fault detection system (see column 6, lines 19-39).

Regarding claim 3,

The method of claim 1, further comprising generating a fault detection index from said measured processing attributes, and forwarding said index to said run-to-run controller for purposes of modifying said at least one setpoint (see column 5, lines 57-67 and column 6, lines 1-3).

Regarding claim 4,

The method of claim 1, wherein said modifying comprises comparing a predicted output against an acceptable tool specification limit (see column 3, lines 39-47).

Regarding claim 5,

The method of claim 1, wherein said modifying comprises comparing a predicted output against an acceptable tool range (see column 3, lines 39-47).

Regarding claim 6,

The method of claim 1, further comprising terminating said processing upon detection of a fault condition (see column 3, lines 49-59).

Regarding claim 7,

The method of claim 1, wherein said at least one setpoint comprises two or more setpoints (see column 5, lines 57-67 and column 6, lines 1-3 along with column 3, lines 39-47).

Regarding claim 8,

The method of claim 1, wherein said at least one setpoint comprises at least one of temperature, pressure, power, processing time, lift position and flow rate of a material (see column 3, lines 39-47).

Regarding claim 9,

The method of claim 1, wherein said fault condition comprises a tool fault (see column 3, lines 39-47).

Regarding claim 10,

The method of claim 1, wherein said fault condition comprises a wafer property fault (see column 3, lines 39-47).

Regarding claim 11,

The method of claim 1, wherein fault detection models used to define a range of conditions indicative of a fault condition are modified to incorporate, as parameters, said at least one setpoint of said recipe at said run-to-run controller (see column 5, lines 24-37, lines 46-67

and column 6, lines 1-47).

Regarding claim 12,

The method of claim 1, wherein said measured wafer properties are not used to modify said recipe when a wafer fault is detected (see column 5, lines 24-37, lines 46-67 and column 6, lines 1-47).

Regarding claim 13,

A method for processing wafers (see column 3, lines 63-67), said method comprising the steps of:

1) processing said wafers according to a recipe, wherein said recipe includes at least one setpoint for obtaining one or more target wafer properties (see column 5, lines 24-37, batch [i.e. wafer-to-wafer or lot-to-lot]);

2) measuring wafer properties (see Figure 1, sensor 115, column 3, lines 5-15);

3) detecting conditions indicative of a fault condition (see column 5, lines 57-67 and column 6, lines 1-3 and column 3, lines 16-19); and

4) modifying said at least one setpoint of said recipe according to said measured wafer properties to maintain said target wafer properties in the absence of a fault condition (see column 6, lines 19-39).

Regarding claim 14,

The method of claim 13, wherein processing is terminated if a fault condition is detected (see column 3, lines 49-59).

Regarding claim 15,

The method of claim 13, wherein said step of measuring occurs during processing (see column 3, lines 39-47).

Regarding claim 17,

The method of claim 13, wherein fault detection models used to define a range of conditions indicative of a fault condition are modified to incorporate, as parameters, said at least one setpoint of said recipe (see column 5, lines 24-37, lines 46-67 and column 6, lines 1-47).

Regarding claim 18,

A system for processing wafers in a manufacturing execution system (see column 3, lines 63-67), said system comprising

a run-to-run controller for controlling a tool according to a recipe received from said manufacturing execution system, wherein said recipe includes at least one setpoint for obtaining one or more target wafer properties (see column 5, lines 24-37, batch [i.e. wafer-to-wafer or lot-to-lot]);

a sensor for measuring processing attributes including wafer properties (see Figure 1, sensor 115, column 3, lines 5-15);

a fault detector for monitoring said wafer properties to detect conditions indicative of a fault condition and forwarding said conditions to said run-to-run controller (see column 5, lines 57-67 and column 6, lines 1-3 and column 3, lines 16-19); and

wherein said at least one setpoint of said recipe is modified according to said processing attributes to maintain said target wafer properties, except when a fault condition is detected by said fault detection system (see column 6, lines 19-39).

Regarding claim 19,

The system of claim 18, further comprising a sensor for measuring wafer properties before execution of processing (see Figure 1, sensor 115, column 3, lines 5-15).

Regarding claim 20,

The system of claim 18, wherein said fault detector generates a fault detection index from said measured processing attributes, and forwards said index to said run-to-run controller for purposes of modifying said at least one setpoint (see column 5, lines 57-67 and column 6, lines 1-3).

Regarding claim 21,

The system of claim 18, wherein said run-to-run controller modifies said at least one setpoint by comparing a predicted output against an acceptable tool specification limit (see column 3, lines 39-47).

Regarding claim 22

The system of claim 18, wherein said run-to-run controller modifies said at least one setpoint by comparing a predicted output against an acceptable tool range (see column 3, lines 39-47).

Regarding claim 23,

The system of claim 18, wherein said run-to-run controller terminates processing upon detection of a fault condition (see column 3, lines 49-59).

Regarding claim 24,

The system of claim 18, wherein said at least one setpoint comprises two or more setpoints (see column 5, lines 57-67 and column 6, lines 1-3 along with column 3, lines 39-47).

Regarding claim 25,

The system of claim 18, wherein said at least one setpoint comprises at least one of temperature, pressure, power, processing time, lift position and flow rate of a material (see column 3, lines 39-47).

Regarding claim 26,

The system of claim 18, wherein said fault condition comprises a tool fault (see column 3, lines 39-47).

Regarding claim 27,

The system of claim 18, wherein said fault condition comprises a wafer property fault (see column 3, lines 39-47).

Regarding claim 28,

The system of claim 18, wherein fault detection models used to define a range of conditions indicative of a fault condition are modified to incorporate, as parameters, said at least one setpoint of said recipe at said run-to-run controller (see column 5, lines 24-37, lines 46-67 and column 6, lines 1-47).

Regarding claim 29,

A system for processing wafers (see column 3, lines 63-67), said system comprising:

a run-to-run controller for processing said wafers according to a recipe, wherein said recipe includes at least one setpoint for obtaining one or more target wafer properties (see column 5, lines 24-37, batch [i.e. wafer-to-wafer or lot-to-lot]);

a sensor for measuring wafer properties (see Figure 1, sensor 115, column 3, lines 5-15);

a fault detector for detecting conditions indicative of a fault condition (see column 5, lines 57-67 and column 6, lines 1-3 and column 3, lines 16-19); and

wherein said run-to-run controller modifies said at least one setpoint of said recipe according to said wafer properties to maintain said target wafer properties in the absence of a fault condition detected by said fault detector (see column 6, lines 19-39).

Regarding claim 30,

The system of claim 29, wherein said run-to-run controller does not modify said at least one setpoint of said recipe if a fault condition is detected (see column 5, lines 24-37, lines 46-67 and column 6, lines 1-47).

Regarding claim 31,

The system of claim 29, wherein said sensor measures wafer properties during processing 9see column 3, lines 39-47).

Regarding claim 33,

The system of claim 29, wherein fault detection models used to define a range of conditions indicative of a fault condition are modified to incorporate, as parameters, said at least one setpoint of said recipe at said run-to-run controller (see column 5, lines 24-37, lines 46-67 and column 6, lines 1-47).

Regarding claim 34,

A system for processing wafers in a manufacturing execution system using a run-to-run controller with a fault detection system (see column 3, lines 63-67), said system comprising:

means for receiving, into said run-to-run controller, a recipe for controlling a tool, wherein said recipe includes at least one setpoint for obtaining one or more target wafer properties (see column 5, lines 24-37, batch [i.e. wafer-to-wafer or lot-to-lot]);

means for monitoring processing of said wafers by measuring processing attributes including wafer properties and fault conditions identified by said fault detection system (see Figure 1, sensor 115, column 3, lines 5-15);

means for forwarding said processing attributes to said run-to-run controller (see column 5, lines 57-67 and column 6, lines 1-3 and column 3, lines 16-19); and

means for modifying said at least one setpoint of said recipe at said run-to-run controller according to said processing attributes to maintain said target wafer properties, except when a fault condition is detected by said fault detection system (see column 6, lines 19-39).

Regarding claim 35,

The system of claim 34, further comprising means for measuring wafer properties before a execution of processing (see Figure 1, sensor 115, column 3, lines 5-15).

Regarding claim 36,

The system of claim 34, further comprising means for generating a fault detection index from said measured processing attributes, and means for forwarding said index to said run-to-run controller for purposes of modifying said setpoints (see column 5, lines 57-67 and column 6, lines 1-3).

Regarding claim 37,

The system of claim 34, wherein said means for modifying comprises means for comparing a predicted output against an acceptable tool specification limit (see column 3, lines 39-47).

Regarding claim 38,

The system of claim 34, wherein said means for modifying comprises means for comparing a predicted output against an acceptable tool range (see column 3, lines 39-47).

Regarding claim 39,

The system of claim 34, further comprising means for terminating said processing upon detection of a fault condition (see column 3, lines 49-59).

Regarding claim 40,

The system of claim 34, wherein said fault condition comprises a tool fault (see column 3, lines 39-47).

Regarding claim 41,

The system of claim 34, wherein said fault condition comprises a wafer property fault (see column 3, lines 39-47).

Regarding claim 42,

The system of claim 34, wherein fault detection models used to define a range of conditions indicative of a fault condition are modified to incorporate, as parameters, said at least one setpoint of said recipe at said run-to-run controller (see column 5, lines 24-37, lines 46-67 and column 6, lines 1-47).

Regarding claim 43,

A system for processing wafers (see column 3, lines 63-67), said system comprising:

means for processing said wafers according to a recipe, wherein said recipe includes at least one setpoint for obtaining one or more target wafer properties (see column 5, lines 24-37, batch [i.e. wafer-to-wafer or lot-to-lot]);

means for measuring wafer properties; means for detecting conditions indicative of a fault condition (see Figure 1, sensor 115, column 3, lines 5-15); and

means for modifying said at least one setpoint of said recipe according to said measured wafer properties to maintain said target wafer properties in the absence of a fault condition (see column 6, lines 19-39).

Regarding claim 44,

The system of claim 43, wherein processing is terminated if a fault condition is detected (see column 3, lines 49-59).

Regarding claim 45,

The system of claim 43, wherein fault detection models used to define a range of conditions indicative of a fault condition are modified to incorporate, as parameters, said at least one setpoint of said recipe at said run-to-run controller (see column 5, lines 24-37, lines 46-67 and column 6, lines 1-47).

Regarding claim 58,

A method for processing items in a manufacturing execution system using a run-to-run controller with a fault detection system (see column 3, lines 63-67), said method comprising the steps of:

1) receiving, into said run-to-run controller, a recipe for controlling a tool, wherein said recipe includes at least one setpoint for obtaining one or more target item properties (see column 5, lines 24-37, batch [i.e. wafer-to-wafer or lot-to-lot]);

2) monitoring processing of said items by measuring processing attributes including item properties and fault conditions identified by said fault detection system (see Figure 1, sensor 115, column 3, lines 5-15);

3) forwarding said processing attributes to said run-to-run controller (see column 5, lines 57-67 and column 6, lines 1-3 and column 3, lines 16-19); and

4) modifying said at least one setpoint of said recipe at said run-to-run controller according to said measured processing attributes to maintain said target item properties, except when a fault condition is detected by said fault detection system (see column 6, lines 19-39).

Regarding claim 60,

The method of claim 58, further comprising generating a fault detection index from said measured processing attributes, and forwarding said index to said run-to-run controller for purposes of modifying said at least one setpoint (see column 5, lines 57-67 and column 6, lines 1-3).

Regarding claim 61,

The method of claim 58, further comprising terminating said processing upon detection of a fault condition (see column 3, lines 49-59).

Regarding claim 62,

The method of claim 58, wherein said at least one setpoint comprises two or more setpoints (see column 5, lines 57-67 and column 6, lines 1-3 along with column 3, lines 39-47).

Regarding claim 63,

A method for processing items (see column 3, lines 63-67), said method comprising the steps of:

1) processing said items according to a recipe, wherein said recipe includes at least one setpoint for obtaining one or more target item properties (see column 5, lines 24-37, batch [i.e. wafer-to-wafer or lot-to-lot]);

2) measuring item properties (see Figure 1, sensor 115, column 3, lines 5-15);

3) detecting conditions indicative of a fault condition (see column 5, lines 57-67 and column 6, lines 1-3 and column 3, lines 16-19); and

4) modifying said at least one setpoint of said recipe according to said measured item properties to maintain said target item properties in the absence of a fault condition (see column 6, lines 19-39).

Regarding claim 64,

The method of claim 63, wherein processing is terminated if a fault condition is detected (see column 3, lines 49-59).

Regarding claim 65,

A system for processing items in a manufacturing execution system (see column 3, lines 63-67), said system comprising:

a run-to-run controller for controlling a tool according to a recipe received from said manufacturing execution system, wherein said recipe includes at least one setpoint for obtaining one or more target item properties (see column 5, lines 24-37, batch [i.e. wafer-to-wafer or lot-to-lot]);

a sensor for measuring processing attributes including item properties (see Figure 1, sensor 115, column 3, lines 5-15);

a fault detector for monitoring said item properties to detect conditions indicative of a fault condition and forwarding said conditions to said run-to-run controller (see column 5, lines 57-67 and column 6, lines 1-3 and column 3, lines 16-19); and

wherein said at least one setpoint of said recipe is modified according to said processing attributes to maintain said target item properties, except when a fault condition is detected by said fault detection system (see column 6, lines 19-39).

Regarding claim 67,

The system of claim 65, wherein said fault detector generates a fault detection index from said measured processing attributes, and forwards said index to said run-to-run controller for purposes of modifying said at least one setpoint (see column 5, lines 57-67 and column 6, lines 1-3).

Regarding claim 68,

The system of claim 65, wherein said run-to-run controller terminates processing upon detection of a fault condition (see column 3, lines 49-59).

Regarding claim 69,

The system of claim 65, wherein said at least one setpoint comprises two or more setpoints (see column 5, lines 57-67 and column 6, lines 1-3 along with column 3, lines 39-47).

Regarding claim 70,

A system for processing items (see column 3, lines 63-67), said system comprising:

a run-to-run controller for processing said items according to a recipe, wherein said recipe includes at least one setpoint for obtaining one or more target item properties (see column 5, lines 24-37, batch [i.e. wafer-to-wafer or lot-to-lot]);

a sensor for measuring item properties (see Figure 1, sensor 115, column 3, lines 5-15);

a fault detector for detecting conditions indicative of a fault condition (see column 5, lines 57-67 and column 6, lines 1-3 and column 3, lines 16-19); and

wherein said run-to-run controller modifies said at least one setpoint of said recipe according to said item properties to maintain said target item properties in the absence of a fault condition detected by said fault detector (see column 6, lines 19-39).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 2,16,32,46-57,59 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller in view of US patent 6,230,069 B1, granted to Campbell et al..

With respect to claims 2,16,32,47,59,66, the patent to Miller discloses all the elements of the claims except for the details about the timing of the measurement of data being done prior to

or after the processing of the semiconductor wafer. The patent to Campbell, see column 3, lines 62-67 and column 4, lines 1-8 provides the benefit of pre-polish thickness and post-polish thickness measurements using metrology tools in a semiconductor manufacturing processing system in order to provide a more efficient manner in which to obtain measurements without providing any delays in the processing system. This would provide more batch processing to be completed in an expeditious manner without any further delays. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the semiconductor manufacturing system of Miller to include pre and post measurements with metrology tools to gain the added benefits mentioned above.

With respect to claims 46-57, the only difference between these claims and the patent to Miller is that the claims of the instant invention are set forth in a computer readable embodiment. It is clear that Miller is using a computer system to control his semiconductor manufacturing system and thus it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the processing steps of Miller to be embodied upon a computer readable medium for operating the semiconductor manufacturing system.

Regarding claim 2,

The method of claim 1, further comprising measuring wafer properties before execution of processing (see column 3, lines 62-67 and column 4, lines 1-8).

Regarding claim 16,

The method of claim 13, wherein said step of measuring occurs after processing (see column 3, lines 62-67 and column 4, lines 1-8).

Regarding claim 32,

The system of claim 29, wherein said sensor measures wafer properties after processing

(see column 3, lines 62-67 and column 4, lines 1-8).

Regarding claim 46,

A computer program embodied on a computer-readable medium for processing wafers in a manufacturing execution system using a run-to-run controller with a fault detection system (see column 3, lines 63-67), said computer readable medium comprising:

computer readable instructions for receiving, into said run-to-run controller, a recipe for controlling a tool, wherein said recipe includes at least one setpoint for obtaining one or more target wafer properties (see column 5, lines 24-37, batch [i.e. wafer-to-wafer or lot-to-lot]);

computer readable instructions for monitoring processing of said wafers by measuring processing attributes including wafer properties and fault conditions identified by said fault detection system (see Figure 1, sensor 115, column 3, lines 5-15);

computer readable instructions for forwarding said processing attributes to said run-to-run controller (see column 5, lines 57-67 and column 6, lines 1-3 and column 3, lines 16-19); and

computer readable instructions for modifying said at least one setpoint of said recipe at said run-to-run controller according to said measured processing attributes to maintain said target wafer properties, except when a fault condition is detected by said fault detection system (see column 6, lines 19-39).

Regarding claim 47,

The computer-readable medium of claim 46, further comprising computer readable instructions for measuring wafer properties before execution of processing (see column 3, lines 62-67 and column 4, lines 1-8).

Regarding claim 48,

The computer-readable medium of claim 46, further comprising computer readable instructions for generating a fault detection index from said measured processing attributes, and computer readable instructions for forwarding said index to said run-to-run controller for purposes of modifying said setpoints (see column 5, lines 57-67 and column 6, lines 1-3).

Regarding claim 49,

The computer-readable medium of claim 46, wherein said computer readable instructions for modifying comprises computer readable instructions for comparing a predicted output against an acceptable tool specification limit (see column 3, lines 39-47).

Regarding claim 50,

The computer-readable medium of claim 46, wherein said computer readable instructions for modifying comprises computer readable instructions for comparing a predicted output against an acceptable tool range (see column 3, lines 39-47).

Regarding claim 51,

The computer-readable medium of claim 46, further comprising computer readable instructions for terminating said processing upon detection of a fault condition (see column 3, lines 49-59).

Regarding claim 52,

The computer-readable medium of claim 46, wherein said fault condition comprises a tool fault (see column 3, lines 39-47).

Regarding claim 53,

The computer-readable medium of claim 46, wherein said fault condition comprises a wafer property fault (see column 3, lines 39-47).

Regarding claim 54,

The computer-readable medium of claim 46, wherein fault detection models used to define a range of conditions indicative of a fault condition are modified to incorporate, as parameters, said at least one setpoint of said recipe at said run-to-run controller (see column 5, lines 24-37, lines 46-67 and column 6, lines 1-47).

Regarding claim 55,

A computer program embodied on a computer-readable medium for processing wafers (see column 3, lines 63-67), said computer-readable medium comprising:

computer readable instructions for processing said wafers according to a recipe, wherein said recipe includes at least one setpoint for obtaining one or more target wafer properties (see column 5, lines 24-37, batch [i.e. wafer-to-wafer or lot-to-lot]);

computer readable instructions for measuring wafer properties (see Figure 1, sensor 115, column 3, lines 5-15);

computer readable instructions for detecting conditions indicative of a fault condition (see column 5, lines 57-67 and column 6, lines 1-3 and column 3, lines 16-19); and

computer readable instructions for modifying said at least one setpoint of said recipe according to said measured wafer properties to maintain said target wafer properties in the absence of a fault condition (see column 6, lines 19-39).

Regarding claim 56,

The computer readable medium of claim 55, wherein processing is terminated if a fault condition is detected (see column 3, lines 49-59).

Regarding claim 57,

The computer-readable medium of claim 55, wherein fault detection models used to define a range of conditions indicative of a fault condition are modified to incorporate, as parameters, said at least one setpoint of said recipe (see column 5, lines 24-37, lines 46-67 and column 6, lines 1-47).

Regarding claim 59,

The method of claim 58, further comprising measuring item properties before execution of processing (see column 3, lines 62-67 and column 4, lines 1-8).

Regarding claim 66,

The system of claim 65, further comprising a sensor for measuring item properties before execution of processing (see column 3, lines 62-67 and column 4, lines 1-8 along with Miller's sensor 115).

Correspondence Information

Any inquiries concerning this communication or earlier communications from the examiner should be directed to **Emanuel Todd Voeltz** who may be reached via telephone at **(703) 305-4563**. The examiner can normally be reached Monday through Friday between the hours of 8:00 a.m. and 5:00 p.m. eastern standard time.

If you need to send an Official facsimile transmission, please send it to **(703) 872-9306**. If you would like to send a Non-Official (draft) facsimile transmission the fax is **(703) 746-5104**. If attempts to

reach the examiner by telephone are unsuccessful, the Examiner's Supervisor, **Anthony Knight**, may be reached at **(703) 308-3179**.

Any response to this office action should be mailed too: **Director of Patents and Trademarks Washington, D.C. 20231**.

Moreover, hand-delivered responses should be delivered to the Receptionist, located on the fo**urth floor of Crystal Park 11, 2121 Crystal Drive Arlington, Virginia**.

Emanuel Todd Voeltz
Primary Patent Examiner
Art Unit 2121
United States Department of Commerce
Patent & Trademark Office

EMANUEL TODD VOELTZ
PRIMARY EXAMINER

Notice of References Cited	Application/Control No. 10/135,405	Applicant(s)/Patent Under Reexamination REISS ET AL.	
	Examiner Emanuel T. Voeltz	Art Unit 2121	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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	B	US-6,268,270 B1	07-2001	Scheid et al.	438/522
	C	US-6,449,524 B1	09-2002	Miller et al.	700/121
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"A real-time equipment monitoring and fault detection system", Guo et al., Semiconductor Manufacturing Technology Workshop, June 16-17, 1998, pps. 111-121.
	V	"Equipment and APC integration at AMD with workstream", Lantz, IEEE International Symposium on Semiconductor Manufacturing Conference Proceedings, October 11-13, 1999, pps. 325-327.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.